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L3: Entry 27 of 157

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TITLE: Parallel access virtual channel memory system

Detailed Description Text (46):

A prefetch command can be issued by a memory master. The prefetch command specifies that a particular row is to be read from a particular one of memory banks 301-304 and loaded into a particular entry of a specified one of the virtual access channels 1-8, via the memory bank interface bus 310. The prefetch command can be executed concurrently with an operation that involves the reading or writing of data between the virtual access channels 1-8 and the memory system interface 314 on the memory system interface bus 312. Furthermore, each of the memory banks 301-304 can be performing separate prefetch operations with respect to different cache entries in different virtual access channels. Of course, these concurrent prefetch operations among the memory banks 301-304 are pipelined (staggered at different phase of operations) by virtue of the fact that the prefetch commands are issued/initiated at different times. Furthermore, the staggered stages of execution also ensure that there is no conflict in the use of the memory bank interface bus 310 in transferring the data from the memory banks 301-304 to the virtual access channels 1-8.

CLAIMS:

9. The method of claim 8, further comprising the step of transferring data between one of the memory masters and one of the virtual access channels concurrently with the step of prefetching data.

10. The method of claim 8, further comprising the step of restoring data from a selected one of the virtual access channels to the memory array in response to a restore command issued by one of the memory masters, wherein the step of restoring data is performed concurrently with the step of prefetching data.

11. The method of claim 1, wherein the memory array comprises a plurality of memory banks, the method further comprising the step of concurrently prefetching data from a plurality of the multiple banks to a corresponding plurality of the virtual access channels in response to a plurality of prefetch commands issued by the memory masters.